IN THE CLAIMS:

Please amend claims 1, 3, 5-14 as follows.

1. (Currently) A method of performing a data transfer between a memory ~~(16)~~ of a processor device ~~(10)~~ and a circuitry ~~(20)~~ connected to said processor device ~~(10)~~, said method comprising the steps of:

a) setting up a direct memory access (DMA) for transferring data at said circuitry ~~(20)~~;

b) triggering a DMA transfer of said data to said processor device ~~(10)~~;

c) adding said DMA transfer to a transaction log;

d) providing said transaction log to said processor device ~~(10)~~, when said transaction log has reached a predetermined depth limit; and

e) informing said processor device ~~(10)~~ of the availability of said transaction log.

2. (Original) A method according to claim 1, wherein said steps b) and c) are repeated until said depth limit has been reached.

3. (Currently Amended) A method according to claim 1 ~~or 2~~, wherein said informing step is performed by initiating an interrupt operation.

4. (Original) A method according to claim 3, wherein said interrupt operation initiates an interrupt service routine.

5. (Currently Amended) A method according to ~~any one of the preceding claims~~ claim 1, further comprising the step of validating said transferred data at said processor device ~~(10)~~ based on said available transaction log.

6. (Currently Amended) A method according to ~~any one of the preceding claims~~ claim 1, wherein said circuitry is an ASIC.

7. (Currently Amended) A method according to ~~any one of the preceding claims~~ claim 1, further comprising the step of storing said transaction log in said memory ~~(16)~~.

8. (Currently Amended) A processor device having a memory ~~(16)~~ which can be accessed by a connected circuitry ~~(20)~~, said processor device ~~(10)~~ being arranged to validate data, transferred to said memory ~~(16)~~ by a direct memory access, based on a transaction log provided to said processor device.

9. (Currently Amended) A processor device according to claim 8, wherein said processor device ~~(10)~~ is arranged to validate said transferred data in response to an interrupt triggered by said connected circuitry ~~(20)~~.

10. (Currently Amended) A processor device according to claim 8 ~~or 9~~, wherein said processor device is a digital signal processor ~~(10)~~.

11. (Currently Amended) An integrated circuit having means ~~(22)~~ for providing access to a processor device ~~(10)~~, said integrated circuit ~~(20)~~ being arranged to set up a

direct memory access (DMA) for transferring data via said access means ~~(22)~~, to trigger a DMA transfer of said data, to add said DMA transfer to said transaction log, to provide said transaction log to said processor device when said transaction log has reached a predetermined depth limit, and to issue an information indicating the availability of said transaction log.

12. (Currently Amended) A integrated circuit according to claim 11, wherein said integrated circuit ~~(20)~~ is arranged to issue said information by triggering an interrupt.

13. (Currently Amended) An integrated circuit according to claim 11 ~~or 12~~, wherein said integrated circuit is an ASIC.

14. (Currently Amended) A system for performing a data transfer between a memory ~~(16)~~ of a processor device ~~(10)~~ and a circuitry ~~(20)~~ connected to said processor device ~~(10)~~,

a) wherein said circuitry ~~(20)~~ is arranged to set up a direct memory access (DMA) for transferring data, to trigger a DMA transfer of said data to said processor device ~~(10)~~, to add said DMA transfer to a transaction log, to provide said transaction log to said processor device ~~(10)~~ when said transaction log has reached a predetermined depth limit, and to inform said processor device ~~(10)~~ of the availability of said transaction log; and

b) wherein said processor device ~~(10)~~ is arranged to validate said transferred data based on said provided transaction log.